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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,257	KOLB ET AL.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 5, and 12 are objected to because of the following informalities:

Applicant recites in claim 1, lines 4-5 that the phrase of "the printed wiring board has ***a cavity*** with one or more openings ***to the surface of the printed wiring board***" is not understood. What does applicant mean of "the printed wiring board has a cavity"? and how far that "the cavity...to the surface of the printed wiring board?

The Merriam Webster's Collegiate Dictionary is well defined "a cavity" means as "***an unfilled space within a mass***", which is means "the cavity is a hole with one end is open and another end is closed. Also, the drawings are just shown the printed circuit board having a space/spacing to contain at least one or more openings on the surface of the printed wiring board (PWB) and did not show the PWB having a cavity.

Examiner suggests to change "a cavity" to –a space--, and the phrase of "the PWB has a cavity with one or more openings to the surface of the PWB" should be –the PWB has a space containing at least one or more openings on the surface of the PWB—because the PWB does not have "a cavity".

Claim 5, line 3, "a component" should be –the component—for proper antecedent basis.

Claim 12, line 6, "the component body" should be –the device body—for proper antecedent basis.

Please, review all of the claims (depending on claim 1) carefully and correct these and any similar errors.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, and 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, line 4, it is confuse. Does applicant recite "a plurality of openings the same of "one or more opening of claim 1, line 4.?

Regarding claim 3, lines 4-5, it is unclear. The phrase of "the volume of space...to the surface of the PCB" is not understood. How far that "the volume of space to the surface of the PCB"? Applicant should clarify this limitation.

Regarding claim 12, lines 3-5, it is confuse. The phase of "a plurality of components, each...formed one or more printed circuit board (PCB) regions having a highly variable and cavitatious surface including at least one cavity" is not understood.

First, which one of "each component or the PCB regions" has a highly variable and cavitatious surface"?

Second, what does applicant mean of "a ***highly variable and cavitatious surface***" applicant should clarify this limitation.

Last, "a highly variable and cavitatious surface including at least one cavity" is unclear. In addition, the Merriam Webster's Collegiate Dictionary is well defined "a cavity" means as "an unfilled space within a mass", which means "the cavity is a hole with one end is open and another end is closed. Applicant defines "the cavity" which is not correct terminology term to apply in the claimed languages, since the drawings are shown "a space or spaces or spacing" between leads of the component or "a space or spaces or spacing" between each of the components formed on the PWB, and the space is not the same the terminology term as the cavity.

Regarding claim 12, lines 6-7, it is unclear. The phrase of "the component body adjacent the component leads and a portion of the PWB below the component leads" is not understood. What does applicant mean "the component body adjacent the component leads and a portion of the PWB below the component leads"? Applicant should clarify this limitation.

Regarding claim 12, lines 7-9, it is unclear. The phrase of "each such cavity...to the surface of the PCB" is not understood. How far that "each such cavity to the surface of the PCB"?

As explained above, examiner suggests to change, "each such cavity...to the surface of the PCB" to –each space...on the surface of the PWB--.

Claim 3 recites the limitation "said component body" in line 3. There is improper antecedent basis for this limitation in the claim.

Please, review all of the claims carefully and correct these and any similar errors.

Note of claim languages

Regarding claim 1, examiner would treats "a cavity having one or more openings to the surface of the printed circuit board (PCB)" in claim 1, lines 4-5 such as "a space containing at least one or more openings on the surface of the PCB.

Regarding claim 1, lines 9-10, examiner would treats "inaccessible to subsequently-applied coatings" such as "intended use" for subsequently-applied coating.

Regarding claim 3, lines 1-2, examiner would treats "the cavity comprises a volume space defined by leads of a component" should be --the volume space that defined underneath between the leads of the component--.

Regarding claim 12, lines 5-8, examiner would treats "at least one cavity defined by component leads, and each such cavity includes a plurality of openings to the surface of the PCB" should be –at least one space defined underneath of the leads of the component--, and –each space includes a plurality of openings on the surface of the PCB--.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1, 3-5, 7, 11-12, 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by McCullough et al. (U. S. Patent 6,127,038).

As to claim 1, McCullough et al. disclose a printed circuit board (PCB, 12-figure 1, column 2, line 37) comprising:

a printed wiring board (PWB 12);

a component (22, column 3, line 1) mounted on said PWB, wherein the PWB has a space with one or more openings on the surface of the PWB (***note***: it should be noted that the space would defined as a space on top and bottom surface of the PWB, spacing that underneath of the leads of the component, or as a space/spacing between each of the components 22 mounted on the PWB 12); and

an electrically non-conductive filler material (14, column 3, lines 8, 52-64) disposed in the space and on the surface of the PWB immediately surrounding the space so as bridge across and to at least partially infill the one or more openings of the space, wherein the filler material renders the cavity substantially *inaccessible to* (*intended use for*) subsequently-applied coatings (16, column 3, line 15).

As to claim 12, McCullough et al. disclose a printed circuit board (PCB, 12-figure 1, column 2, line 37) comprising:

a printed wiring board (12);

a plurality of components (22, column 3, line 1), each having a device body mounted on said PWB to form one or more PCB regions having a surface including at least one space (*see the note in claim* 1) defined by component leads, wherein each

space includes at least one opening (underneath of component 22 or between the components) on the surface of the PWB; and

a layer of non-electrically-conductive filler material (14, column 3, lines 8, 52-64) adhered to the PCB surface in at least one of the one or more regions to provide a contoured, contiguous filler material surface having gradual transition, wherein the filler material at least partially infills the at least one space and bridge across the at least one space so as to encapsulate and seal the space (top and bottom surfaces of the PWB, underneath of leads of the component, or space between the components).

As to claims 3 and 5, McCullough et al. disclose the PCB (12) wherein the space comprises a volume of space define by leads (24), column 3, line 2, (the volume of space is underneath of the leads of the component), of the components (22) and the PWB, wherein the volume of space defined by the space on the surface of the PCB between neighboring component leads (24).

As to claim 4, McCullough et al. disclose the PCB wherein the space comprises a volume of space between neighboring components (22) mounted on the PCB.

As to claims 7 and 14, McCullough et al. disclose the PCB wherein said filler material is an epoxy (column 3, line 34).

As to claim 11, McCullough discloses the subsequently-applied coating (16) comprises a layer of dielectric coating that conformingly coats exposed surfaces of the PWB, the component, and the filler material (14), wherein the openings of the space are sufficiently large to prevent the dielectric coating from bridging across the openings of the space without the presence of the filler material.

As to claim 15, McCullough et al disclose the PCB further comprising a low viscosity, high adherence dielectric coating (16) that, when applied and cured, covers predetermined portions of said PCB including at least a portion of the one or more regions coated with sad filler material (14), wherein the filler material (14) prevents the dielectric coating (16) from entering the at least one space.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 8-10, 13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCullough et al. (U. S. Patent 6,127,038) in view of Kotani et al. (JP 200034457 A, hereafter JP).

As to claim 6, 9, 13, and 17, McCullough et al. do not disclose all of the limitations of the claimed invention; except for the filler material is thixotropic and thermally cured epoxy.

Kotani et al. (JP) shows a high-pressure resistant thixotropic epoxy resin adhesive (see abstract) including a thermally cured epoxy.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ thixotropic epoxy resin including a thermally cured epoxy in the PCB of McCullough, as taught by Kotani et al. (JP) for the purpose of retaining a

sufficient adhesion thickness under high bearing pressure and maintaining a strength at temperature that applied on the surface of the PCB.

As to claim 8, McCullough et al. do not disclose said epoxy is one of the family of Bisphenol-A epoxies mixed with an amine hardner.

Kotani et al. (JP) shows a epoxy resin is one of the family of Bisphenaol-A epoxies mixed with an amine harder (see pages 2-3 of the translation).

It would have been obvious to one of ordinary skill in the art at the invention was made to employ a epoxy resin is one of the family of Bisphenaol-A epoxies mixed with an amine harder in the PCB of McCullough, as taught by Kotani et al. for purpose of providing a stiffness and high temperature performance.

As to claim 10, McCullough et al. do not disclose said epoxy be a latex based non-electrically conductive epoxy. Kotani et al. shows a epoxy resin that is a latex based non-electrically conductive composition (see pages 2-3 of the translation).

It would have been obvious to one of ordinary skill in the art at the invention was made to employ a epoxy resin is a latex based non-electrically conductive epoxy in the PCB of McCullough, as taught by Kotani et al. for purpose of providing a high resistance to damage from moisture and high temperature performance.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over McCullough et al. (U. S. Patent 6,127,038) in view of Higgins, III (U. S. Patent 5,639,989).

As to claim 16, McCullough et al. do not disclose the PCB further comprising a conductive coating covered the dielectric coating layer.

Higgins, III shows a conductive coating (62; 64, column 9, lines 53-67) covered a dielectric coating layer (60-figure 3).

It would have been obvious to one of ordinary skill in the art at the invention was made to employ a conductive coating covered a dielectric coating in the PCB of McCullough, as taught by Higgins, III for purpose of providing ground shielding potential to the PCB.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 3-17 have been considered but are moot in view of the new ground(s) of rejection.

Applicant 's arguments are not persuasive. Applicant argues that "McCullough fails to achieve its purpose of providing a conformal coating comprised of two coating layers (14, 16) applied to all exposed surfaces on the PCB including surfaces of the components and leads, and including between and behind lead surfaces." It is incorrect. McCullough clearly discloses a conformal coating and a method for applying to a PCB (see the abstract, and column 1, lines 5-10), the conformal coating (14 or 16) is provided to coat on the surfaces of the PCB (20), components (22) and leads (24) of the components. Therefore, McCullough clearly discloses the purpose of the conformal coating to the PCB.

Further, applicant argues McCullough comprised a first coating layer (14) that does not bridging across "cavity openings" to encapsulate and seal "cavities"

Examiner disagrees. McCullough clearly discloses in figure 1 that the first coating layer (14) does bridging across the space (see the note in claim 1) to encapsulate and seal the space.

Applicant argues that McCullough comprised the first coating layer (14) that does not render "a cavity" substantially inaccessible to subsequently-applied coating. Examiner disagrees. McCullough clearly discloses the first coating that renders the space (see the note in claim 1), and the word "inaccessible to subsequently-applied coating" which is "intended use" for further in use to the next coating or does not require the next coating on the first coating.

Therefore, examiner believes the Office action is proper and including all of the limitations of the claimed languages.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Frederickson et al., Nepcon West documents, and Lee et al. disclose related art.

Nepcon West documents discloses a conformal coating applying on a surface of a printed circuit board, Ferderickson et al. discloses a conformal coating (24) bridging across spaces on the surface of the PCB, and Lee et al. discloses a conformal coating

(40) bridging across spaces on the surface of the PCB. Three references cited read on all the limitations in claims 1 and 12.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
April 30, 2004.

Luan Thai
Primary Examiner

4/30/04